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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,694	07/16/2004	Renatus Josephus Van Der Vleuten	NL020029US	2762
24738 7	10/06/2006	EXAMINER		
	ECTRONICS NORTH	MOON, SEOKYUN		
INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ		ART UNIT	PAPER NUMBER	
SAN JOSE, C			2629	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

			Application	No.	Applicant(s)				
Office Action Summary		10/501,694		VAN DER VLEUTEN ET AL.					
		Examiner		Art Unit					
			Seokyun Mo		2629				
Period fo	The MAILING DATE of this commu r Reply	nication appe	ears on the c	over sheet with the c	orrespondence ad	idress			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).									
Status				•					
1) 又	Responsive to communication(s) fil	ed on 21 Jui	ly 2006.						
· —	This action is FINAL . 2b) ☐ This action is non-final.								
,	Since this application is in condition	for allowan	ice except for	r formal matters, pro	secution as to the	e merits is			
,	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
4)⊠	Claim(s) 1-10 is/are pending in the	application.							
-	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)	5) Claim(s) is/are allowed.								
6)⊠	6)⊠ Claim(s) <u>1-10</u> is/are rejected.								
-	Claim(s) is/are objected to.								
8)□	Claim(s) are subject to restri	ction and/or	r election req	uirement.					
Applicati	on Papers								
9)[The specification is objected to by the	ne Examiner	r.						
10)⊠	The drawing(s) filed on 16 July 2004	<u>4</u> is/are: a)[∑	accepted o	or b) objected to b	by the Examiner.				
	Applicant may not request that any obje	ection to the o	drawing(s) be	neld in abeyance. See	e 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11)	11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority (ınder 35 U.S.C. § 119		·			•			
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).									
a)⊠ All b)□ Some * c)□ None of:									
	1. Certified copies of the priority documents have been received.								
	2. Certified copies of the priority documents have been received in Application No								
	3. Copies of the certified copies of the priority documents have been received in this National Stage								
	application from the International Bureau (PCT Rule 17.2(a)).								
* See the attached detailed Office action for a list of the certified copies not received.									
Attachment(s)									
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review ((DTO-048)	4	4) Interview Summary (PTO-413) Paper No(s)/Mail Date					
3) Information Disclosure Statement(s) (PTO/SB/08) 5) Notice of Informal Patent Application									
Paper No(s)/Mail Date 6) Other:									

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DETAILED ACTION

Specification

1. The specification was objected for missing title for each part of the specification.

Currently, the specification is amended.

The objection of the specification has been withdrawn.

Claim Objections

2. Claim 1 was objected for a minor spelling error.

Currently, the claim is amended.

The objection of claim 1 has been withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

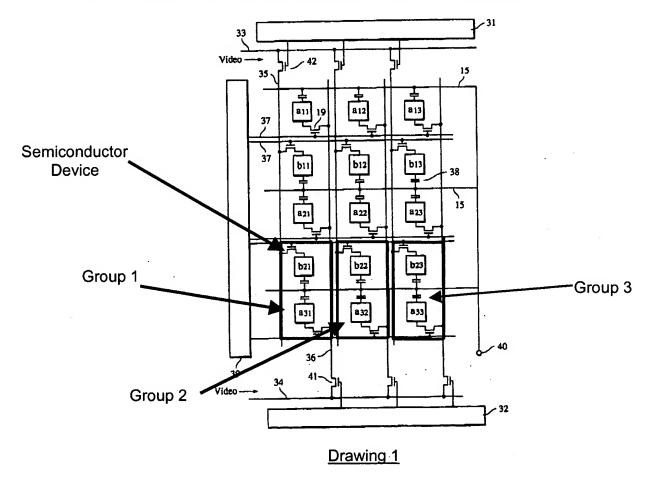
- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1-3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi (US Pat. No. 5,721,596) in view of Kasai et al. (US Pat. No. 6,587,120 B2, herein after referred to as "Kasai").

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As to **claim 1**, Kochi teaches a display device ("active matrix liquid crystal display device") comprising:

a substrate, the substrate is provided with groups of pixels wherein each group of pixels is within a separate defined area (the rectangles drawn on drawing 1) on the substrate [abstract lines 1-8] [drawing 1 provided on page 3 of this Office action, which is equivalent to Kochi's figure 3]; and

a plurality of semiconductor devices, ("pixel transistors") wherein each semiconductor device is mainly associated with a different group of pixels, and wherein each semiconductor device is positioned within the defined area of the group of pixels that it is mainly associated with [drawing 1], the semiconductor device being provided with drive means for driving pixels dependent on data to be displayed.



Kochi does not teach picture scaling means.

However, Kasai [fig. 7] teaches picture scaling means ("data converters 24, 25, and 26") used to convert the resolution of data signals representing images to be displayed in a display device [col. 1 lines 33-36].

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Kasai's picture scaling means in Kochi's display device to implement a function of accepting an interface signal having a resolution different from that of display device and thus to display data contained in the interface signal regardless of the resolution of the display data [col. 1 lines 47-52].

As to **claim 2**, Kochi modified by Kasai [Kasai: figs. 7 and 11] teaches the picture scaling means (Kasai: "data converters 24, 25, and 26") to comprise means (Kasai: "resolution switching mean 57") to determine the kind of scaling (Kasai: whether to receive inputs of "reduced display data 55" or "enlarged display data 56") to be performed [Kasai: col. 8 lines 30-33].

As to **claim 3**, Kochi modified by Kasai inherently teaches the picture scaling means to provide several pixels within a group of pixels with the same voltage since it is required for adjacent pixels in groups to display same content of images when an image with a low resolution is displayed on a display having a higher resolution, and thus it is required to provide same voltages to the adjacent pixels to display same content of images.

As to claim 10, Kochi [fig. 3] teaches the drive means to have a bus structure ("scanning bus lines 33 and 34" and "data bus lines 35 and 36") [col. 7 lines 30-35].

6 Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi and Kasai as applied to claims 1-3 above, and further in view of Nomura et al. (US Pat. No. 4,866,520, herein after referred to as "Nomura").

As to claim 4, Kochi modified by Kasai does not teach the picture scaling means to determine intermediate voltages for neighboring pixels.

However, Nomura [fig. 1] teaches picture scaling means (a combination of "interpolator 22" and "selector 24") determining intermediate voltages ("interpolated voltage") for adjacent lines of pixels ("selector 24" cyclically selects among even, odd, and interpolated lines of data for display) [col. 2 lines 41-49 and abstract].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the modified Kochi's picture scaling means to implement Nomura's interpolator and selector to provide interpolated voltage for neighboring pixels, which achieves the increment of the number of lines of pixels per picture [abstract lines 9-10], and thus provides an improved method for converting video signals of a first resolution to video signals of another resolution [col. 2 lines 15-17].

As to claims 5 and 6, Kochi modified by Kasai and Nomura teaches the picture scaling means determining intermediate voltages for pixels in neighboring lines.

The modified Kochi does not expressly disclose the adjacent lines to be rows or columns.

However, the adjacent lines applied with the intermediate voltages are to be rows when the picture scaling is performed or executed in vertical direction and thus the image to be displayed expands to upper and lower area of the display. On the other hand, the adjacent lines applied with the intermediate voltages are to be columns when the picture scaling is performed or executed in horizontal direction and thus the image expands to left and right side area of the display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the modified Kochi's adjacent lines of pixels provided with intermediate voltages to be rows or columns depending on the direction that the image to be displayed expands when the picture scaling is executed.

As to claim 7, Kochi [fig. 3] teaches a connection ("scanning bus lines 37") between neighboring semiconductor devices.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi, Kasai, Nomura, and further in view of Anwyl et al. (US Pat. No. 5,576,738, herein after referred to as "Anwyl").

Kochi teaches the driving means to comprise a frame memory [col. 7 lines 38-42].

Kochi does not teach the driving means to comprise means to detect changes between the contents of subsequent frames.

However, Anwyl [fig. 3] teaches a driving mean (a combination of "activity detector 403", "microprocessor 402", "timer 405", and "memory 404") for a display comprising a mean ("activity detector 403") to detect changes between the contents of subsequent frames [col. 1 lines 37-43].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the structure of Kochi's driving circuit to include means detecting changes between the contents of subsequent frames, as taught by Anwyl, in order to allow Kochi's display to detect changes between the contents of subsequent frames, thus to provide power management function in the display device [col. 1 lines 45-59 and col. 4 line 58- col. 5 line 17].

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi and Kasai as applied to claims 1-3 above, and further in view of Takeda (US Pat. No. 4,903,013, herein after referred to as "Takeda").

Kochi modified by Kasai does not expressly disclose the means for recognizing the location to have a read-only memory.

However, Takeda [fig. 1] teaches a display system having a plurality of display areas having RAM (which is a programmable memory) as an addressing mean [abstract].

It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the modified Kochi's means for recognizing the location to comprise RAM since RAM is a known storage device providing large memory while requires less space to build on electronic circuits.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 18, 2006

S.M.

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SUPERVISORY PATENT EXAMINED